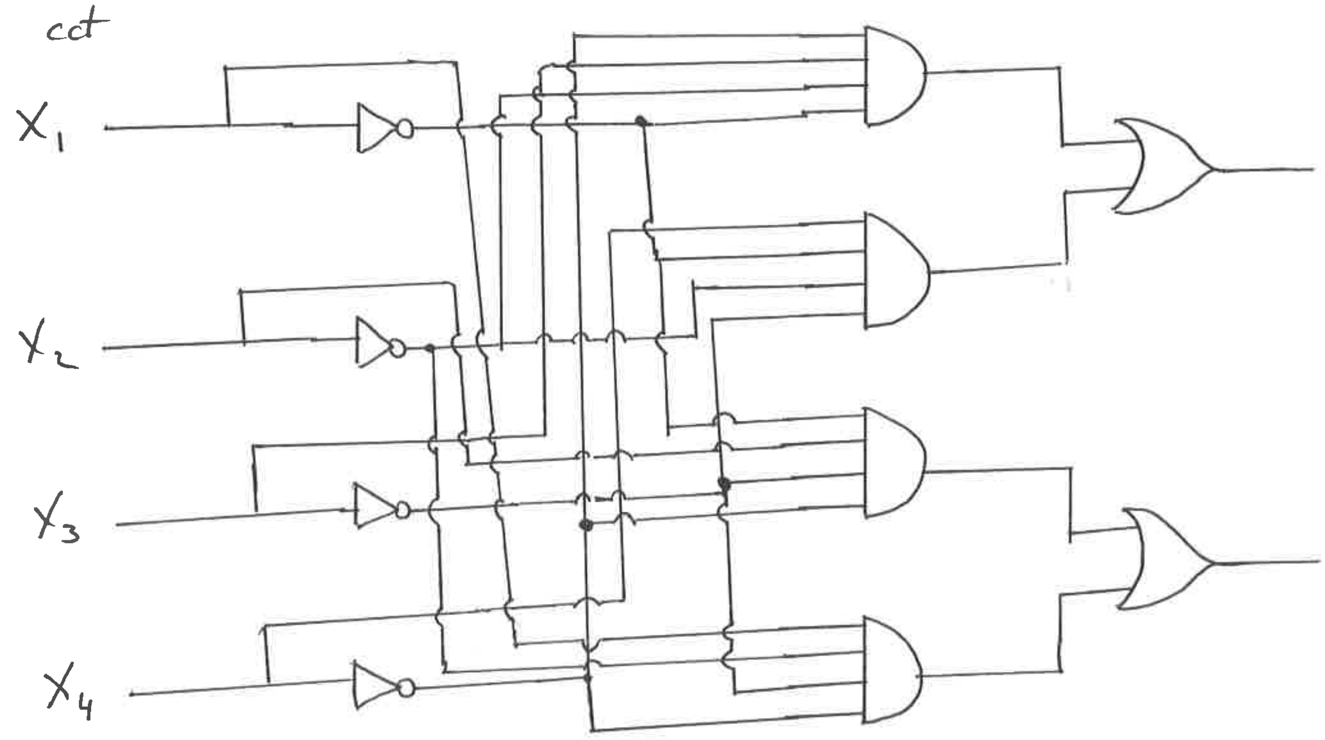
Logic cct



(4-2 Encoder)

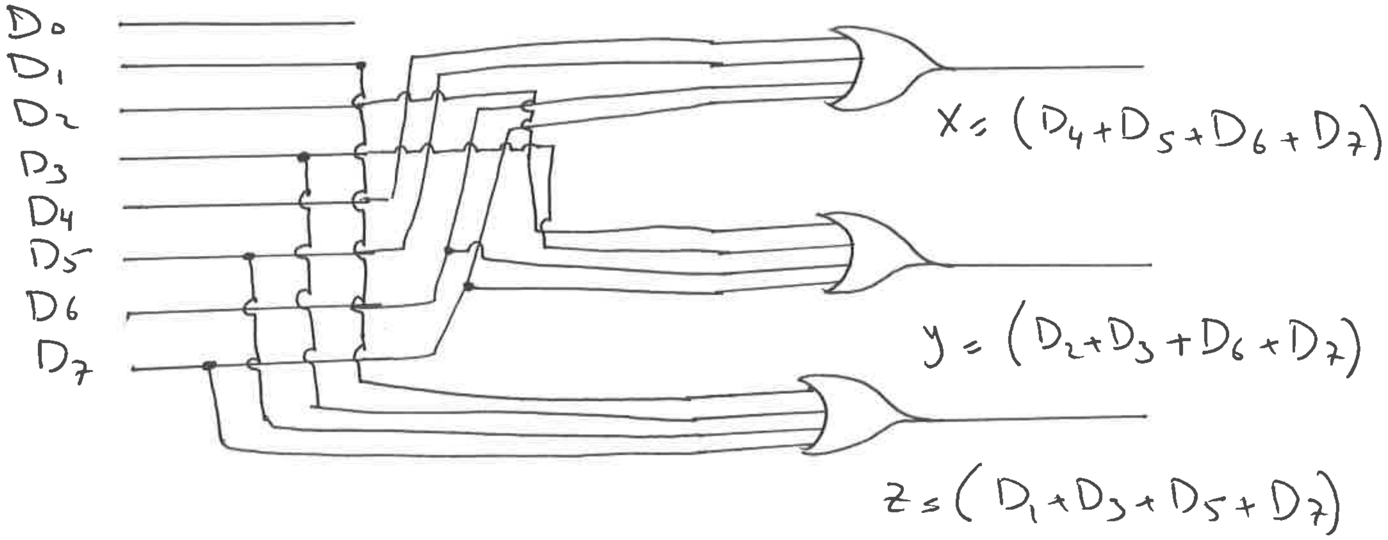
Ex) By using Encoder, Design octat-to-Binary Encoder?

I/P								O/P		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$x = \sum 4, 5, 6, 7$

$y = \sum 2, 3, 6, 7$

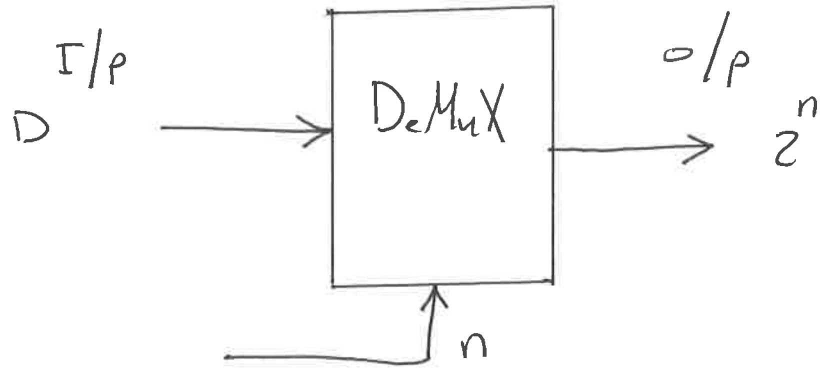
$z = \sum 1, 3, 5, 7$



(octal-to-Binary encoder)

DeMultiplexer :-

A demultiplexer (DMuX) basically reverses the multiplexing Function. It takes data from one line and distributes them to agiven number of output line.



The Simple type of DeMultiplexer is (1-2) line DeMuX and the number of Select line is n.

In general, there are $(1-2^n)$ line DMuX, and the number of Select lines is n.

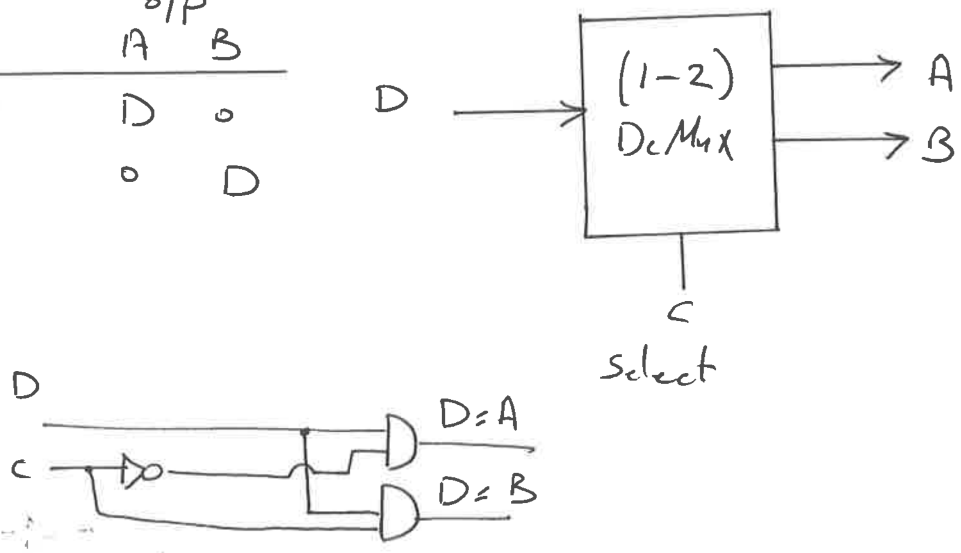
Ex) Design (1-2) DeMux Circuit?

i/p	o/p	
C	A	B
0	D	0
1	0	D

$A = \bar{C}D$

$B = CD$

Logic cct :--



Ex) Design (2-4) D MUX circuit?

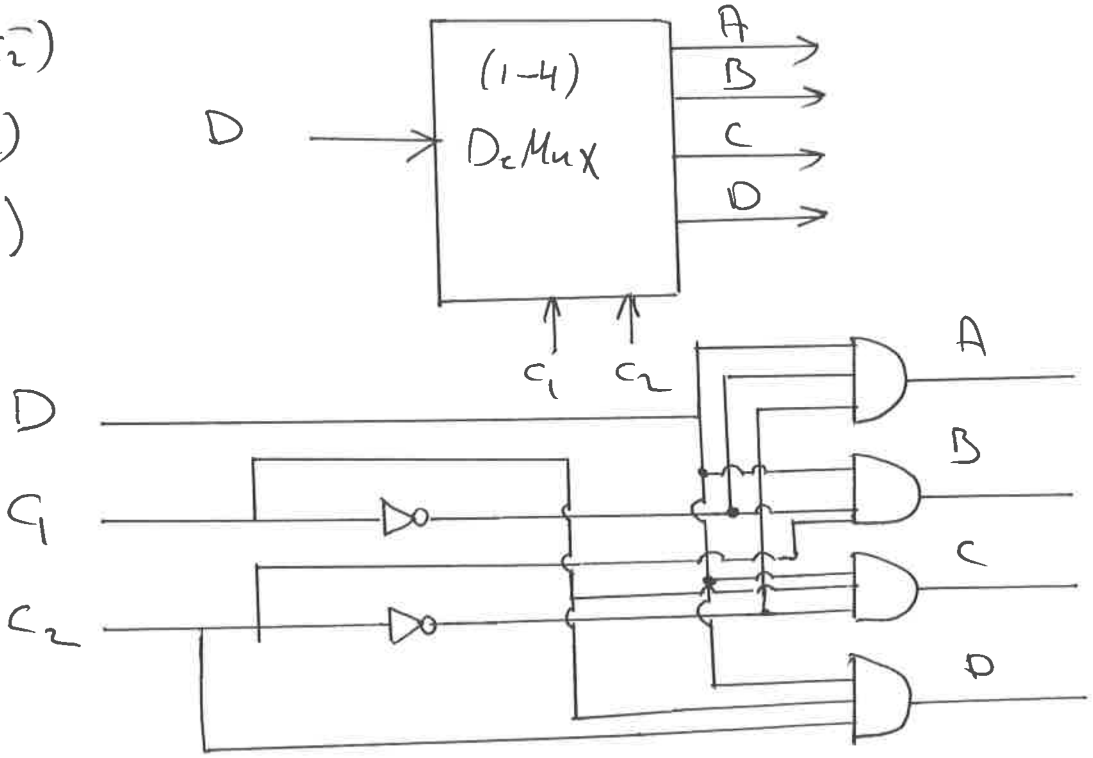
i/p		o/p			
C_1	C_2	A	B	C	D
0	0	D	0	0	0
0	1	0	D	0	0
1	0	0	0	D	0
1	1	0	0	0	D

$A = D(\bar{c}_1\bar{c}_2)$

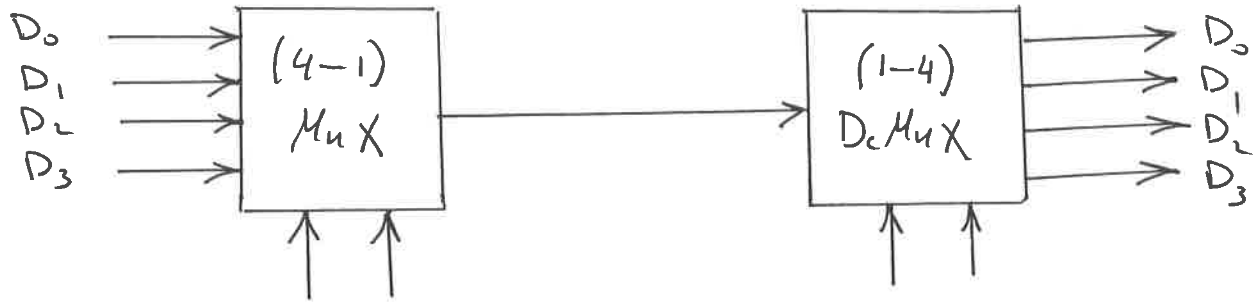
$B = D(\bar{c}_1\bar{c}_2)$

$C = D(c_1\bar{c}_2)$

$D = D(c_1 c_2)$

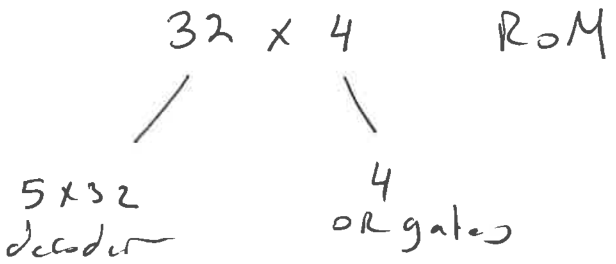


Ex) Design (4-1) MuX and (1-4) line DeMuX circuit?

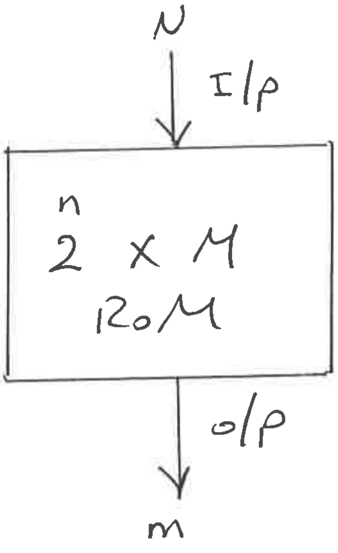


Read only Memory (RoM):—

which is adevice that Includes both the (decoder) and (OR) gates with in a Single Ic package.



It is amemory (or storage) device in which a fixed set of binary Information stored, there is n input lines and m output lines.



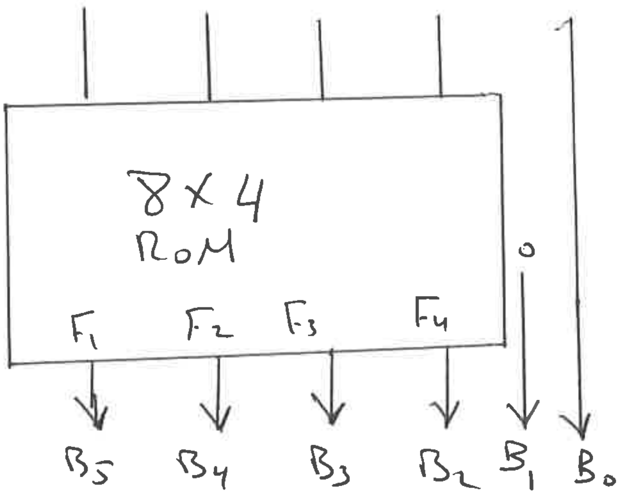
(Block Diagram & RoM)

Ex) Design a combinational Circuit using a RoM. The cct accept 3 bit number and generats output binary number equal to the square of the input number?

Sol^n)

I/p			o/p						
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

(Block Diagram of RoM)



RoM truth table

A_2	A_1	A_0	F_1	F_2	F_3	F_4
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

* This truth table for RoM, from this T.T, we Can Design the Internal cct for the RoM. ((H.W))

Types of RoMs:-

The RoM may be programmed in two different ways.

First:- Is called mask programming and is done by the mannfactuer during the last fabrication process of the unit and called RoM.

Second:- (PROM)

where PRoM units contain all 0's (or all 1's) in every bit of the stored words. The links in the PRoM are broken by application of current pulses through the output terminals. A broken link. defin a binary and unbroken defines another state and these type is irreversible.

Third:-

Is called EPRoM which can change in aspecial altraviolet light for agiven period of time.

The RoM is can be Viewed or interprted in two different ways:-

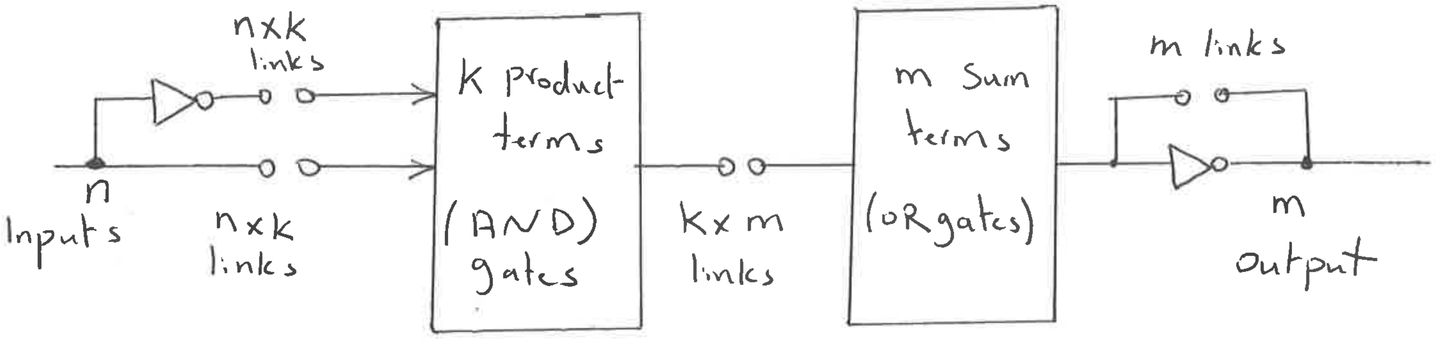
1) The first as function Implementer.

2) The Second as storage device.

Programable Logic Array (PLA) :-

This device, we use it to reduce the Logic cct's that we use to design more then functions, by matching between the terms for each function as fellow:-

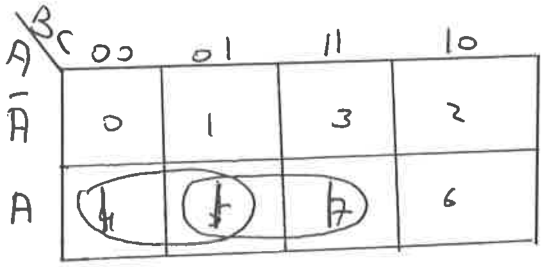
Block Diagram:-



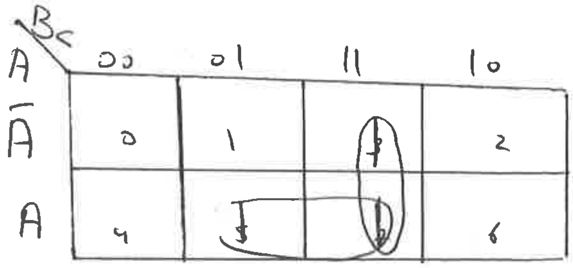
(PLA Block Diagram)

Ex) Implement the truth table using PLA ?

A	B	C	F_1	F_2
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	0	0
1	1	1	1	1



$F_1 = A\bar{B} + AC$



$F_2 = BC + AC$

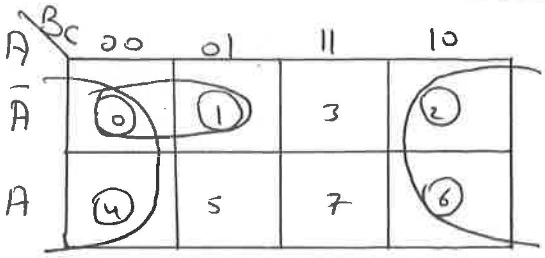
$F_1 = A\bar{B} + AC$

$\bar{F_1} = \overline{A\bar{B} + AC}$

$= (\bar{A}+B)(\bar{A}+\bar{C})$

$= \bar{A} + \bar{A}\bar{C} + \bar{A}B + B\bar{C}$

$= \bar{A} + B\bar{C}$



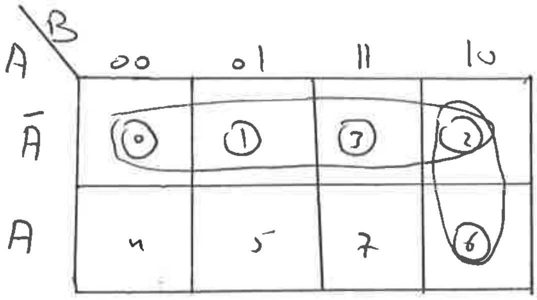
$\bar{F_2} = \bar{C} + \bar{A}\bar{B}$

$F_2 = AC + BC$

$\bar{F_2} = \overline{AC + BC}$

$= (\bar{A}+\bar{C})\cdot(\bar{B}+\bar{C})$

$= \bar{A}\bar{B} + \bar{C}$



$\bar{F_1} = \bar{A} + B\bar{C}$

Hences:-

* $\boxed{F_1 = A\bar{B} + AC}$

$\bar{F_1} = \bar{A} + B\bar{C}$

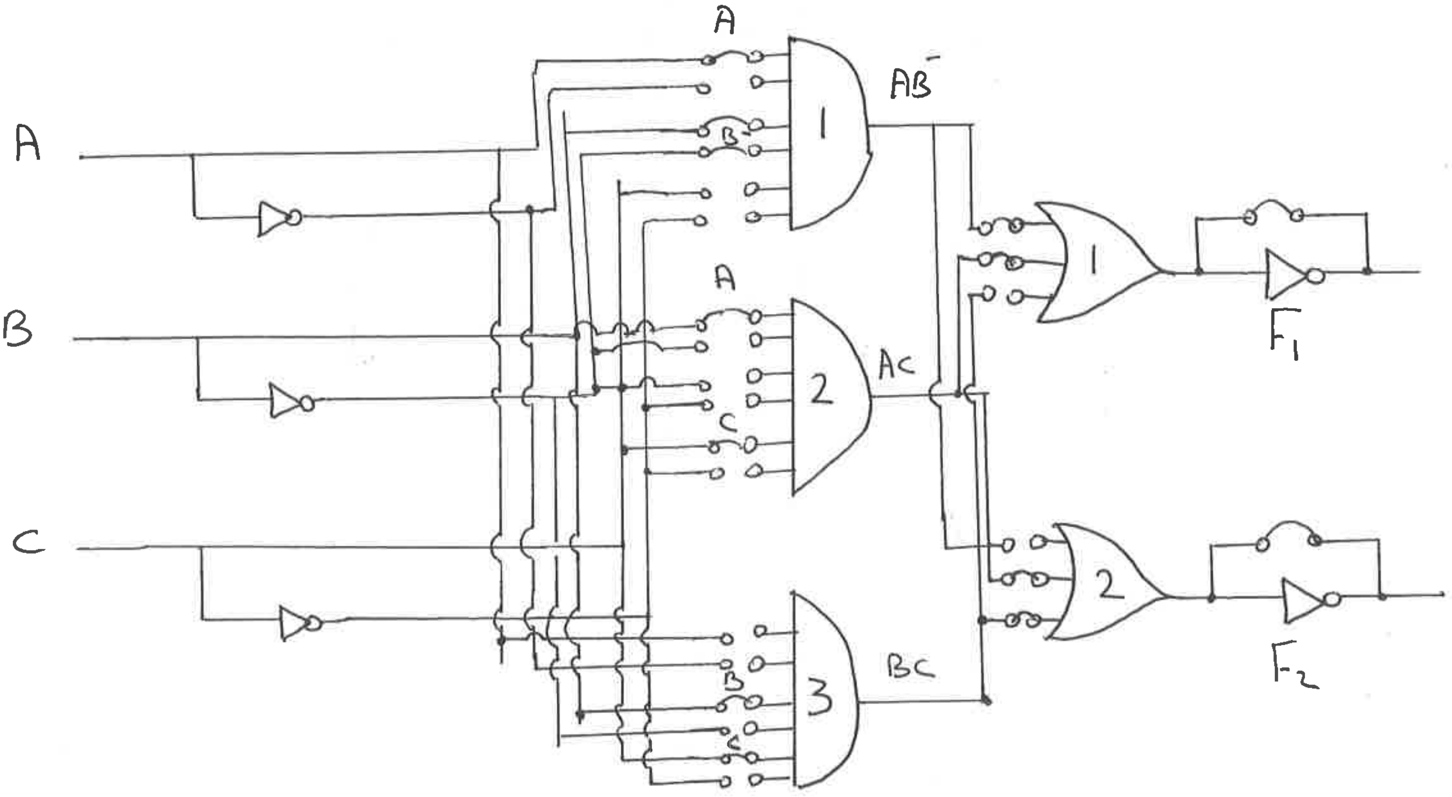
* $\boxed{F_2 = AC + BC}$

$\bar{F_2} = \bar{A}\bar{B} + \bar{C}$

We choose F_1 & F_2

product term	Inputs			outputs	
	A	B	C	F_1	F_2
$A\bar{B}$	1	0	—	1	—
AC	1	—	1	1	1
BC	—	1	1	—	1
				T	T

The Logic cct :-



« Logic cct »

Ex) A combinational circuit is defined by the functions

$$F_1(A,B,c) = \Sigma(3,5,6,7)$$

$$F_2(A,B,c) = \Sigma(0,2,4,7)$$

Implement the circuit with a pLA having three inputs, four product term and two outputs?

Sol)

A	B	C	F_1	F_2
0	0	0	0	1
0	0	1	0	0
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A \ BC	00	01	11	10
$\bar{A}$	0	1	3	2
A	4	5	7	6

$F_1 = AC + AB + BC$

A \ BC	00	01	11	10
$\bar{A}$	0	1	3	2
A	4	5	7	6

$\bar{F_1} = \bar{B}\bar{C} + \bar{A}\bar{C} + \bar{A}\bar{B}$

A \ BC	00	01	11	10
$\bar{A}$	0	1	3	2
A	4	5	7	6

$F_2 = \bar{B}\bar{C} + \bar{A}\bar{C} + ABC$

A \ BC	00	01	11	10
$\bar{A}$	0	1	3	2
A	4	5	7	6

$\bar{F_2} = \bar{B}C + \bar{A}C + AB\bar{C}$

Hence:-

$$F_1 = AC + AB + BC$$

$$\boxed{\bar{F_1} = \bar{B}\bar{C} + \bar{A}\bar{C} + \bar{A}\bar{B}}$$

$$\boxed{F_2 = \bar{B}\bar{C} + \bar{A}\bar{C} + ABC}$$

$$\bar{F_2} = \bar{B}C + \bar{A}C + AB\bar{C}$$

We choose $\bar{F_1}$ & F_2 :-

PLA program table:-

product term		Inputs			outputs	
		A	B	C	F_1	F_2
1	$\bar{B}\bar{C}$	—	0	0	1	1
2	$\bar{A}\bar{C}$	0	—	0	1	1
3	$\bar{A}\bar{B}$	0	0	—	1	—
4	ABC	1	1	1	—	1
					C	T